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TSMC-03-636

April 30, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/812,729 03/30/04

Hsien-Ping Feng et al.

POST ECP MULTI-STEP ANNEAL/H2 TREATMENT TO REDUCE FILM IMPURITY

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 4, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B. Ackerman 5/4/04

U.S. Patent 6,380,084 to Lim et al., "Method to Form High Performance Copper Damascene Interconnects by De-Coupling Via and Metal Line Filling," discloses a method to form robust dual damascene interconnects by decoupling via and connective line trench filling.

U.S. Patent 6,582,569 to Chiang et al., "Process for Sputtering Copper in a Self Ionized Plasma," describes a self ionized plasma (SIP) method for sputtering copper.

U.S. Patent Application Publication US 2003/0140988 A1 to Gandikota et al., "Electroless Deposition Method Over Sub-Micron Apertures," discusses a catalytic layer of a noble or semi-noble metal deposited on a seed layer to patch any discontinuities.

U.S. Patent 6,077,780 to Dubin, "Method for Filling High Aspect Ratio Openings of an Integrated Circuit to Minimize Electromigration Failure," discusses a copper seed layer deposited in an opening and annealed above 200 degrees C to reflow the copper seed layer and minimize the number of seams or grain boundaries in the layer.

U.S. Patent 6,245,670 to Cheung et al., "Method for Filling a Dual Damascene Opening Having High Aspect Ratio to Minimize Electromigration Failure," discusses a via in a dual damascene structure filled by an electroless plating process.

U.S. Patent 6,391,777 to Chen et al., "Two-Stage Cu Anneal to Improve Cu Damascene Process," discloses a two stage copper anneal to improve reliablilty of a copper damascene interconnect.

U.S. Patent 6,350,688 to Liu et al., "Via RC Improvement for Copper Damascene and Beyond Technology," discloses an anneal procedure that is applied to copper damascene via interconnects after copper ECP deposition and prior to copper planarization.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-03-636	10/812,729
Applicant: Hsien-Ping Feng et al.	
Filing Date: 03/30/04	Group Art Unit

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6380084	4/30/02	Lim et al.	438	687	10/2/00
	6582569	6/24/03	Chiang et al.	204	192.17	10/10/00
	6077780	6/20/00	Dubin	438	687	12/3/97
	6245670	6/12/01	Cheung et al.	438	637	2/19/99
	6391777	5/21/02	Chen et al.	438	687	5/2/01
	6350688	2/26/02	Liu et al.	438	687	8/1/00

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

*	US Patent App. Publication US 2003/0140988 A1 to
*	Gandikota et al., Pub. Date 07/31/03, Filed 01/28/02,
*	US Cl. 148/527.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.